Claims

1. A semiconductor memory comprising:

a plurality of memory cells arranged in a matrix array;

a plurality of bit line pairs each thereof being connected to each column of the plurality of the memory cells;

a plurality of sense amplifiers of each connected to each bit line pair ;

a plurality of first gate pairs;

a plurality of second gate pairs;

a plurality of first data line pairs of each to be connected with one of the bit line pairs selected by means of the first gate pairs, on activation; and

a plurality of second data line pairs of each to be connected with the first data line pair by means of the second gate pairs; wherein

the first data line pair and the second data line pair are arranged to intersect each other.

2. A semiconductor memory comprising:

a plurality of memory cells arranged in a matrix array;

a plurality of bit line pairs each thereof being connected to each column of the plurality of the memory cells;

a plurality of sense amplifiers of each connected to each bit line pair ;

a plurality of first gate pairs;

a plurality of second gate pairs;

a plurality of first data line pairs of each, laid on said memory cell, to be connected with one of the bit line pairs selected by means of the first gate pairs, on activation; and

a plurality of second data line pairs of each, laid on the memory cells,

to be connected with one of the first data line pairs by means of the second gate pairs; wherein

the first data line pair and the second data line pair are arranged to intersect with each other.

3. The semiconductor memory according to claim 1 or 2, wherein said first and second gate pairs are layouted in the outer space of a memory cell array.

4. A semiconductor memory comprising:

a plurality of memory cells arranged in a matrix array;

a plurality of bit line pairs each thereof being connected to each column of the plurality of the memory cells;

a plurality of sense amplifiers of each connected to each bit line pair ;

a plurality of first gates;

a plurality of second gates;

a plurality of first data lines of each to be connected with one line of one of the bit line pairs of selected by means of the first gates, on activation; and

a plurality of second data lines of each to be connected with one of the first data lines by means of the second gates; wherein

the first data line and the second data line are arranged to intersect each other.

5. A semiconductor memory comprising:

a plurality of memory cells arranged in a matrix array;

a plurality of bit line pairs each thereof being connected to each column of the plurality of the memory cells;

a plurality of sense amplifiers of each connected to each bit line pair ;

a plurality of first gate pairs;

a plurality of second gate pairs;

a plurality of first data line pairs of each, laid on said memory cell, to be connected with one of the bit line pairs selected by means of the first gate pairs, on activation

a plurality of first data line pairs of each to be connected on a time sharing basis with one of the bit line pairs selected by means of the first gate pairs, on activation; and

a plurality of second data line pair pairs of each to be connected with the first data line pairs of each by means of the second gate pairs; wherein

the first data line pair and the second data line pair are arranged to intersect each other.

6. A semiconductor memory comprising:

one or a plurality of processor elements having arithmetic functions;

a plurality of memory cells arranged in a matrix array;

a plurality of bit line pairs each thereof being connected to each column of the plurality of the memory cells;

a plurality of sense amplifiers of each connected to each bit line pair ;

a plurality of first gate pairs;

a plurality of second gate pairs;

a plurality of first data line pairs of each to be connected with one of the bit line pairs selected by means of the first gate pairs, on activation; and

a plurality of second data line pairs to be connected with one of the first data line pairs by means of the second gate pairs; wherein

the first data line pair and the second data line pair are arranged to intersect each other.

7. A semiconductor memory comprising:

one or a plurality of processor elements;

a plurality of memory cells arranged in a matrix array;

a plurality of bit line pairs each thereof being connected to each column of the plurality of the memory cells;

a plurality of sense amplifiers of each connected to each bit line pair ;

a plurality of first gates;

a plurality of second gates;

a plurality of first data lines of each to be connected with one line of one of the bit line pair of a column selected by means of the first gates, on activation; and

a plurality of second data lines of each to be connected with one of the first data lines by means of the second gates; wherein

the first data line and the second data line are arranged to intersect each other.

8. A semiconductor memory comprising:

one or a plurality of processor elements;

a plurality of memory cells arranged in a matrix array;

a plurality of bit line pairs each thereof being connected to each column of the plurality of the memory cells;

a plurality of sense amplifiers of each connected to each bit line pair ;

a plurality of first gates;

a plurality of second gates;

a plurality of first data line pairs of each to be connected on a time sharing basis with one of the bit line pair selected by means of the first gate pair, on activation; and

a plurality of second data line pair to be connected with the first data lines pair by means of the second gate pairs; wherein

the first data line pair and the second data line pair are arranged to

intersect each other.

9. A semiconductor memory comprising:

a plurality of processor elements;

a plurality of memory cells arranged in a matrix array and organized into a plurality of memory block groups;

a plurality of bit line pairs each thereof being connected to each column of the plurality of the memory cells;

a plurality of sense amplifier connected to each bit line pair ;

a plurality of first gate pairs;

a plurality of second gate pairs;

a plurality of first data line pairs of each to be connected with one of the bit line pairs selected by means of the first gate pairs, on activation; and

a plurality of second data line pairs of each to be connected with one of the first data line pairs by means of the second gate pairs; wherein

the first data line pair and the second data line pair are arranged to intersect each other.

10. A semiconductor memory comprising:

a plurality of processor elements;

a plurality of memory cells arranged in a matrix array and organized into a plurality of memory block groups;

a plurality of bit line pairs each thereof being connected to each column of the plurality of the memory cells;

a plurality of sense amplifiers of each connected to each bit line pair ;

a plurality of first gates;

a plurality of second gates;

a plurality of first data lines to be connected with one of the one line of the bit line pairs of a column selected by means of the first gates, on

activation; and

a plurality of second data lines to be connected with the first data lines by means of the second gates; wherein

the first data line and the second data line are arranged to intersect each other.

11. A semiconductor memory comprising:

one or a plurality of processor elements;

a plurality of memory cells arranged in a matrix array and organized into a plurality of groups;

a plurality of bit line pairs each thereof being connected to each column of the plurality of the memory cells;

a plurality of sense amplifiers of each connected to each bit line pair ;

a plurality of first gate pairs;

a plurality of second gate pairs;

a plurality of first data line pairs of each to be connected on a time sharing basis with one of the bit line pairs selected by means of the first gate pairs, on activation; and

a plurality of second data line pairs of each to be connected with one of the first data line pairs by means of the second gate pairs; wherein

the first data line pair and the second data line pair are arranged to intersect each other.

12. The semiconductor memory according to claims 6 to 11, wherein said one or a plurality of processor elements have means for performing data communications with said second data line or data line pair.

13. The semiconductor memory according to claims 6 to 11, said memory further comprising a plurality of control means for controlling a plurality of memory cells organized into one or a plurality of memory block

groups, wherein said control means each have a control signal for controlling each of the groups.

14. The semiconductor memory according to claim 6 to 11, wherein said control means is part of said plurality of processor elements.

15. The semiconductor memory according to claims 6 to 11, wherein Nth input-output data line of said processor elements is to be connected to N-th of said first gate and corresponding N-th said first data line, and those of each N-th arrangement is assigned to N-th partial chunk out of said plurality of bit line pairs, each thereof being connected to each column of the plurality of the memory cells, with a number of column of the product of M neighbor bit line pairs by N chunk.

16. A method for controlling a semiconductor memory comprising the steps of:

requesting for data communications by processor elements which make data communications with a plurality of memory cells organized into memory block groups;

controlling data communications in response to the requests for data communications; and

making data communications between the processor elements and the memory cells in accordance with the control signals under the control, wherein, in the step of controlling communications, control signals for controlling each of a plurality of memory cells organized into individual groups are used .